Claims

1. Circuit arrangement for determining the average value of an input signal (s) with

a signal input (1, 14) for receiving the input signal (s) and

a signal output (13) for outputting an output signal (g, Q_1 ... Q_{n+m}) indicating the average value of the input signal (s),

a counter (10) or a summing unit being arranged between the signal input (1, 14) and the signal output (13) for averaging, said counter being connected on the input side to a comparator (5),

characterized in that

a switching element (6) is arranged in a feedback loop and activated by the output of the comparator (5) to switch to a first reference signal (Pos_Ref) or a second reference signal (Neg_Ref) as a function of the output of the comparator (5).

2. Circuit arrangement according to Claim 1, characterized in that the summing unit or counter (10) is connected on the input side to a sigma-delta modulator (2).

3. Circuit arrangement according to Claim 2, characterized in that the sigma-delta modulator (2) has an adding unit (3) or a subtracting unit, an integrator (4) and a comparator (5) and a feedback loop from the output of the comparator (5) to the

input of the adding unit (3) or subtracting unit.

4. Circuit arrangement according to at least one of the preceding Claims,
characterized in that
the summing unit or counter (10) has a clock input (CLOCK), at which a clock signal (CLK) with a predefined clock frequency is present.

5. Circuit arrangement according to Claim 4,
characterized in that
the input signal (s) is band-limited and has a predefined limit frequency, the clock frequency being a whole-number multiple of the limit frequency.

6. Circuit arrangement according to at least one of the preceding Claims,
characterized in that
the summing unit or counter (10) has a reset input (RESET), at which a control signal (CTRL) is present, the control signal (CTRL) and the input signal (s) having the same fundamental frequency and/or the same phase angle and/or a constant phase relationship to each other.

7. Circuit arrangement according to Claim 6,
characterized in that
the clock signal (CLK) and the control signal (CTRL) have a temporally constant phase relationship to each other.

8. Circuit arrangement according to at least one of the preceding Claims,
characterized in that

the summing unit or adding unit or counter (10) is connected on the output side to an output register (12).

9. Circuit arrangement according to Claim 8, characterized in that
the output register (12) has a control input (LATCH) to control the receipt of data, the control signal (CTRL) being present at the control input (LATCH).